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Attorneys for Defendant Romi Omar Mayder, an individual, Wesley Mayder, an individual, Silicon Test Systems, Inc. a California Corporation, Silicon Test Solutions, LLC.

**UNITED STATES DISTRICT COURT**  
**NORTHERN DISTRICT OF CALIFORNIA**  
**SAN JOSE DIVISION**

VERIGY US, INC, a Delaware Corporation

Plaintiff,

vs.

ROMI OMAR MAYDER, an individual,  
WESLEY MAYDER, an individual,  
SILICON TEST SYSTEMS, INC. a  
California Corporation, SILICON TEST  
SOLUTIONS, LLC, a California Limited  
Liability Corporation, inclusive,

Defendants.

Civil Case No.: C07-04330 RMW (HRL)

**DECLARATION OF ROMI OMAR  
MAYDER**

Date: November 9, 2007

Time: 9:00

Dept.: Judge: Hon. Judge Whyte

HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY

DOCUMENT SUBMITTED UNDER SEAL

Redacted version for public filing

1 I, Romi Omar Mayder, declare as follows:

2 1. I am a defendant in this case and have personal knowledge of the all facts set forth in this  
3 declaration and, if called upon to testify in this Court as to those facts, my testimony would be as  
4 stated herein.

5 Personal History

6  
7 2. I began employment with Hewlett Packard on June 15, 1998, after being hired away from  
8 Schlumberger. In 2000 Agilent spun off from Hewlett Packard and I continued employment with  
9 Agilent. On June 1, 2006 Verigy spun off from Agilent and I continued employment with Verigy  
10 until September 21, 2006, at which time I terminated employment.

11 3. While working for Agilent, I reported to Bob Pochowski, who was general manager of  
12 Agilent's Memory Test Division. In September of 2005 Mr. Pochowski left Agilent to pursue other  
13 career opportunities.

14 Semiconductor Wafer Testing Overview

15  
16 4. Testing During Wafer Sort: Flash memory wafers are tested by inserting them into a memory  
17 tester. Memory testers, such as those manufactured by Verigy and Teradyne, are large  
18 electromechanical test equipment that send electrical signals to the memory device (called the Device  
19 Under Test or DUT). The electrical signals write a pattern of ones and zeros into each memory cell  
20 and then read each back to ensure that the pattern received was identical to the pattern originally  
21 written. If the pattern is not identical, the test fails and the die marked "bad."

22  
23 5. At the highest level, memory test systems have three components: a memory tester; a probe  
24 card; and the DUT (here, a wafer). The memory tester consists of a system bay, test head, and wafer  
25 prober. A pattern of signals is programmed at the system bay, and the signals are electrically sent  
26 through the test head. The test head contains processors for executing test patterns, local memory for  
27

1 storing those test patterns, and switches so that individual signals can be routed from one input to  
 2 multiple or different outputs. The test head interfaces with a wafer by connecting to a probe card. The  
 3 probe card transfers the electrical signals to the wafer under test. The wafer prober holds the wafer  
 4 that will be tested. When the probe card properly aligns with, and contacts the wafer, and the  
 5 programmed electrical signals begin to test the DUT, it is called a "touchdown." The fewer number  
 6 of touchdowns necessary to test an entire wafer, the lower the cost of testing the DUTs. Similarly, the  
 7 greater the number of DUTs that can be tested with a single touchdown the lower the cost of test  
 8 ("COT").

10 6. While there are many kinds of memory, of interest here are NAND flash memory and NOR  
 11 flash memory. These two types of flash memory have some distinct performance and application  
 12 differences.

13 7. For NOR flash memory this write/read pattern testing must be fast and virtually flawless to  
 14 ensure proper working of the DUT. NAND flash memory is less demanding regarding speed of the  
 15 tester and the accuracy of the test. NAND flash is ideal for high capacity, low reliability, data storage  
 16 (such as needed in digital cameras), while NOR flash is best used for low capacity, high reliability  
 17 (such as cell phone information). NOR flash allows for random access to the data. In other words,  
 18 the data contained at any single memory address can be individually retrieved via a parallel interface.  
 19 NAND flash does not allow for random access to data because information is retrieved in large  
 20 blocks (such as 1024 to 2048 bytes) via a serial interface.

22 8. More sophisticated testing resources are required to test NOR flash (than NAND flash  
 23 memory) because of (1) the extremely fast read cycle; and (2) the high number of pins used to  
 24 individually address each memory storage cell. The read cycle time of less than 8 nanoseconds for  
 25 NOR memory forces testing equipment to operate within extremely short time cycles. For example,  
 26

1 [REDACTED]  
 2 [REDACTED] Since each NOR memory cell is individually readable the device must have 32 or 64  
 3 pins dedicated to addressing. In contrast, NAND memories require only 8 pins to read the memory  
 4 cells. This four or eight fold increase in the number of address pins requires tester equipment with  
 5 four to eight times the number of channels to test the device.  
 6

#### 7 Gaining Efficiency In Wafer Sort Testing

8 9. As mentioned above, the greater the number of DUTs tested with a single touchdown, the  
 9 lower the COT. Since memory testers are large expensive machines their tester channels are  
 10 sometime referred to as a "resource." In order to gain more efficiency from this "resource" circuits  
 11 are put on the probe card so that the tester resource is offloaded, or "shared," so that a greater number  
 12 of DUTs can be tested simultaneously. This mounting of circuits on probe cards is sometimes  
 13 referred to as *probe card resource sharing*.  
 14

15 10. In its simplest form a *probe card resource sharing* circuit consists of a circuit that simply fans  
 16 out the test signal from the memory tester to two or more DUTs. This form of resource sharing is  
 17 called fan out, because the signals "fan-out" to two or more DUTs simultaneously.  
 18

19 11. In a more sophisticated example of *probe card resource sharing*, the probe card includes a  
 20 semiconductor switch which not only fans-out, but also selectively transmits the test signals from the  
 21 memory tester to the wafer. This is commonly referred to as *multiplexing*. The switches can be  
 22 implemented with electrical relays or field effect transistors ("FETS"). A multiplex circuit allows  
 23 tester resources to be fanned out to multiple DUTs, while maintaining the uniqueness of each DUT,  
 24 and the ability to disconnect failing DUTs.  
 25

26 12. *Multiplex probe card resource sharing* circuits have been and are currently being practiced by  
 27 memory manufacturers such as Micron and [REDACTED]. They have also been developed by probe card  
 28

vendors such as Form Factor Inc. To the extent that probe card resource sharing circuits increase the number of DUTs simultaneously tested, it reduces the number of tester channels that memory manufacturers need to purchase from memory tester manufacturers such as Verigy and Teradyne.

The [REDACTED] and [REDACTED] Projects

Business Focus

13. [REDACTED]

14. [REDACTED]

Technical Focus

15. [REDACTED]

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(1) [REDACTED]

(2) [REDACTED]

(3) [REDACTED]

(4) [REDACTED]

16. [REDACTED]

17. [REDACTED]

18. [REDACTED]

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[REDACTED]

19. [REDACTED]

The [REDACTED] of [REDACTED]

20. [REDACTED]

21. [REDACTED]

22. On June 1, 2006 the Memory Test Division of Agilent “spun off,” forming its own company  
named Verigy. I continued in my same engineering position.

Beginning a Relationship with Mr. Pochowski

1 23. After notification of the [REDACTED] I contacted Bob Pochowski, the ex general  
2 manager of the Agilent Memory Test Division, to investigate what commercial opportunities might  
3 exist for "probe card resource sharing" products. Even after terminating from Agilent, I observed Mr.  
4 Pochowski regularly meeting with Verigy management. He appeared to be a trusted advisor to the  
5 remaining Agilent management team.

6  
7 24. I was told by Edmundo DeLa Puente (Verigy's Master Design Engineer) that he and Mr.  
8 Pochowski regularly discussed technical research and development information, including the  
9 product roadmap. Mr. Pochowski informed me that he discussed Verigy business issues with Alan  
10 Hart while running at Ranch San Antonio at 11:30am every Thursday. Mr. Pochowski also informed  
11 me that had lunch with Gayn Erickson (the Verigy General Manager of Memory Test) regularly and  
12 they discussed the Verigy product roadmap. Due to these representations I trusted that Mr.  
13 Pochowski understood the status of Verigy's projects and that he remained loyal to Verigy.

14  
15 25. [REDACTED]  
16 [REDACTED]  
17 [REDACTED]

18 26. I felt that there would be no competition with Verigy because these custom chips were  
19 complementary, or adjacent, to Verigy's Memory chip tester business. [REDACTED]  
20 [REDACTED]

21 [REDACTED] I assumed they would also be willing to do so with any new business Mr. Pochowski and I  
22 formed.

23  
24 27. In discussions with Bob Pochowski, he informed me that many memory chip manufacturers  
25 were already building some types of probe card resource sharing in house (San Disk, Samsung,  
26 Hynix), or hiring other companies (Formfactor, TouchDown Technologies, and TSE) to work with  
27

1 them in developing custom probe card resource sharing products. We felt that this could be a business  
 2 opportunity for us also.

3 28. [REDACTED]  
 4 [REDACTED]  
 5 [REDACTED]

6 Pochowski my understanding was that the [REDACTED]  
 7 and that [REDACTED]

8 [REDACTED] I believed it did not contain any Verigy trade secrets,  
 9 and therefore did not mark it confidential.

10 29. It appeared to me that others at Verigy did not consider much of the information I shared with  
 11 Mr. Pochowski confidential, as all but one of the documents (the [REDACTED]) were not  
 12 marked Confidential. I did not remove any confidentiality markings from documents before sending  
 13 them to Mr. Pochowski, and believed that confidential documents were marked as such to ensure  
 14 compliance with the standard CDA.  
 15

16 (1) As shown in the declaration of Ken Hanh Duc Lai, Exhibit A, the [REDACTED]  
 17 [REDACTED] is not marked Confidential.

18 (2) As shown in the declaration of Ken Hanh Duc Lai, Exhibits B, C, and D, the  
 19 [REDACTED]  
 20 are not marked Confidential.

21 (3) As shown in the declarations of Ira Leventhal and Andrew Lee (exhibit A and  
 22 exhibit B respectively to those declarations) the [REDACTED]  
 23 [REDACTED] is not marked Confidential.  
 24

25 30. Although in Verigy's complaint it shows a version of the [REDACTED] that is  
 26 marked Agilent Confidential, that very same document when viewed in the default mode of  
 27

Microsoft Word does not show that marking. A true and correct copy of this view taken from the file sent to [REDACTED]

[REDACTED] is shown in Exhibit D.

31. I did not believe the information I shared with Mr. Pochowski was Verigy Confidential because information contained in those documents appear to all be available from public sources and generally known in the industry.

(1) The [REDACTED] (as shown in the declaration of Ken Hanh Duc Lai, Exhibit A), identifies the [REDACTED]. These specifications are generally obtainable from public datasheets, which specify the pinout and electrical characteristics of the NAND flash memory.

(2) As shown in the declaration of Ken Hanh Duc Lai, Exhibits B, C, and D, the

[REDACTED]

This information is shared by tester manufacturers with every customer so that they can use that information to properly test their specific DUTs. Customers are permitted to share this information with other vendors who help complete the testing process, such as probe card manufacturers.

(3) As shown in the declarations of Ira Leventhal and Andrew Lee (exhibit A and exhibit B respectively) the [REDACTED]

[REDACTED] Specifications for SP4T switches can be easily found on the web from multiple vendors, including Honeywell.

Good Faith Preparations for Leaving Verigy

1 32. On June 15, 2006 I registered the domain name "silicontests.com" with networksolutions.com  
2 in preparation to start my own business.

3 33. After [REDACTED] project, and in preparation for establishing STS, [REDACTED]  
4 [REDACTED]  
5 [REDACTED]  
6 [REDACTED]  
7 [REDACTED]  
8 [REDACTED]  
9 [REDACTED]

10 34. [REDACTED]  
11 [REDACTED]  
12 [REDACTED]  
13 [REDACTED]  
14 [REDACTED]  
15 [REDACTED]  
16 [REDACTED]  
17 [REDACTED]

18 35. On September 8, 2006 I filed a certificate of incorporation on behalf of Silicon Test Solutions,  
19 LLC with the Secretary of State of California, with myself as President. At the time of forming STS I  
20 did not believe that I would compete with Verigy.

21 36. At about this time I informed Verigy management that I had decided to leave Verigy to  
22 pursue other career opportunities. They requested that before leaving that I conduct a "knowledge  
23 transfer" of information known to me that would be useful for Verigy to be successful in its future  
24 business. [REDACTED]  
25 [REDACTED]  
26 [REDACTED]  
27 [REDACTED]

1 [REDACTED] I worked long hours  
 2 my last two weeks at Verigy, despite having a newborn child at home.

3 37. On Wednesday, September 20, 2006 I conducted an exit interview with my manager Preet  
 4 Paul Singh. At this time I returned all Verigy electronic devices to Mr. Singh. I also returned all  
 5 Verigy confidential information that was known to me. I returned my security badge, as well, thus  
 6 eliminating my ability to access anything in the building without specific Verigy authorization. I  
 7 ceased doing any additional work related to my employment for Verigy at this time. My last day of  
 8 salary payment was September 21, 2006. A true and correct copy of my last pay stub is attached as  
 9 Exhibit A.  
 10

11 Post Verigy Efforts – A Complete Change of Target Customer

12 38. I never spoke with any potential customers for the STS Flash Enhancer product before  
 13 terminating with Verigy. My first potential customer meeting was with [REDACTED] who was introduced  
 14 to me by Bob Pochowski. I did speak with potential suppliers such as [REDACTED] (and to a lesser  
 15 degree [REDACTED]) before leaving Verigy, regarding the feasibility of manufacturing an integrated  
 16 circuit for a startup business, such as STS.  
 17

18 39. [REDACTED]  
 19 [REDACTED]

20 40. Soon after terminating employment with Verigy, Alan Hart, a Verigy manager, asked if I  
 21 would consult with the company on writing intellectual property disclosures for Verigy patent  
 22 applications. I agreed to help and was compensated for each disclosure that I completed. I was never  
 23 asked to sign a Confidentiality or Non Disclosure Agreement during these consulting efforts. During  
 24 this time Verigy sent me confidential information in order to complete the disclosures. I destroyed or  
 25  
 26  
 27

1 returned any of the confidential information related to these applications after I was finished with the  
2 information that I was aware of. I was paid [REDACTED] as compensation for these efforts.

3 41. On or about October 31, 2006, I became a consultant for [REDACTED] - a probe  
4 card company. [REDACTED]  
5 [REDACTED]  
6 [REDACTED]  
7 [REDACTED]

8 42. After termination from Verigy I began visiting potential customers to discuss their needs for  
9 probe card resource sharing solutions. I met with as many potential customers as I could to  
10 understand their testing needs. I never talked with any Verigy customers or potential Verigy  
11 customers, or potential STS customers before terminating with Verigy. For example:

12 (1) I first met with [REDACTED]  
13 [REDACTED]  
14 [REDACTED]

15 (2) I first met with [REDACTED]  
16 [REDACTED]  
17 [REDACTED]

18 (3) I first I met with [REDACTED]  
19 [REDACTED]  
20 [REDACTED]

21 (4) I first met with [REDACTED]  
22 [REDACTED]  
23 [REDACTED]

24 43. [REDACTED]  
25 [REDACTED] NOR flash memory testing, rather than  
26 NAND flash memory testing, which requires a much different technical solution. [REDACTED]  
27 [REDACTED]  
28 [REDACTED]

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1 [REDACTED]  
2 [REDACTED]  
3 [REDACTED]  
4 44. To create a custom product for NOR flash memory manufacturers the chip would require a  
5 very sophisticated design and manufacture. One that I had never considered before. One that:

- 6 (1) Would switch between read and write cycles must faster using only the Chip  
7 enable line of the DUTs.  
8  
9 (2) Would need to operate at much higher frequencies.  
10  
11 (3) Would need to support a much higher number of address, data, and control lines  
12 since NOR Memory is fully addressable.  
13  
14 (4) Would allow the chip testers to automate control using only a single tester  
15 channel, with a pulse width modulation input ability.  
16  
17 (5) Would generate very little heat due to wafer temperatures already at 150 degrees  
18 Celsius.  
19  
20 (6) Would have less output capacitance, in the range of 20 micro farads, down from  
21 the original 50 micro farads contemplated for NAND flash memory.  
22  
23 (7) Would require many more selectable switch configurations.  
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25 (8) These changes were significant and [REDACTED]  
26 [REDACTED]  
27 [REDACTED]

28 45. [REDACTED]

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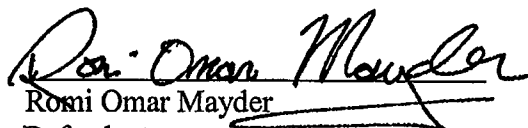
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I declare, under penalty of perjury under the laws of the State of California, the foregoing is true and correct. Executed this 11<sup>th</sup> Day of October, 2007 in San Jose, California.

  
Romi Omar Mayder  
Defendant

# EXHIBIT A

**EXHIBIT FILED  
UNDER SEAL**

# EXHIBIT B

**EXHIBIT FILED  
UNDER SEAL**

# EXHIBIT C

**EXHIBIT FILED  
UNDER SEAL**

# EXHIBIT D

**EXHIBIT FILED  
UNDER SEAL**

# EXHIBIT E

**EXHIBIT FILED  
UNDER SEAL**

# EXHIBIT F

**EXHIBIT FILED  
UNDER SEAL**